Comparison of V^2I_C control with Voltage Mode and Current Mode controls for high frequency (MHz) and very fast response applications

P. Alou, J. A. Oliver, V. Šviković, O. García and J. A. Cobos

Abstract—**High switching frequencies (several MHz) allow the integration of low power DC/DC converters. Although, in theory, a high switching frequency would make possible to implement a conventional Voltage Mode control (VMC) or Peak Current Mode control (PCMC) with very high bandwidth, in practice, parasitic effects and robustness limits the applicability of these control techniques. This paper compares VMC and CMC techniques with the V^2I_C control. This control is based on two loops. The fast internal loop has information of the output capacitor current and the error voltage, providing fast dynamic response under load and voltage reference steps, while the slow external voltage loop provides accurate steady state regulation. This paper shows the fast dynamic response of the V^2I_C control under load and output voltage reference steps and its robustness operating with additional output capacitors added by the customer.**

I. Introduction

Nowadays, power supplies for feeding microprocessors and portable devices demand fast dynamic response. An important disadvantage of implementing a linear control is the need of a high bandwidth to achieve fast dynamic response. This high bandwidth is limited either by the switching frequency or by the robustness to component tolerances of the system. Well known non-linear strategies are V^2 ([1], [2] and [3]) or hysteretic control of the output voltage [3]. Both require sensing the output voltage ripple, which is very small compared to the DC value and it is very sensitive to parasitic effects. It is also required to have a triangular output ripple given by a dominant ESR in the output capacitor.

The non-linear and linear control scheme proposed in [4] is based on a hysteretic control of the output capacitor current of a Buck converter. It achieves a faster control action under load steps since the output capacitor current reacts instantaneously. The problem is to measure the output capacitor current but it can be estimated with the non-invasive method described in [5]. However, this control technique suffers some limitations: variable frequency and high sensitivity to current sensor mismatches.

V^2I_C control proposed in [6] overcomes these limitations and provides very fast response. It is based on the peak current mode control of the output capacitor current that provides very fast dynamic response under load steps, working as a feed-forward of the load current ([7], [8] and [9]). Information of the error between the reference voltage and the output voltage is added to the fast loop to achieve also very fast response under steps in the reference voltage.

In this paper, the V^2I_C control is compared with the conventional Voltage Mode control (VMC) and Peak Current Mode control (PCMC) since these control techniques can provide very high bandwidth when the converter operates at very high frequency (several MHz). The comparison is focused on 1) response under load steps, 2) response under voltage steps, 3) output impedance, 4) line regulation (response under input voltage steps) and 5) robustness and stability issues when external capacitors are added to the output.

II. V^2I_C Control: Operation Principle

The V^2I_C control [6] is based on two loops, a fast internal loop and a slow external loop (Figure 1). It is called V^2I_C control since the output voltage is used in both fast and slow loops (V^2) and the output capacitor current (i_C) is also used in the fast loop.

The control signal (Ctrl) obtained in the fast loop is the addition of: 1) the estimation of the output capacitor current obtained with the simple and non-invasive sensor described in [5], 2) the error between the voltage reference (V_{ref}) and the output voltage (V_{out}) and 3) a compensating slope. This control signal is compared with the reference (Ref) obtained in the slow external loop at the output of a voltage regulator.

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The modulator is a peak mode control and therefore a compensating slope is needed to avoid sub-harmonic oscillations over 50% duty cycles. The compensating slope not only avoids sub-harmonic oscillations, but also helps to desensitize this technique to current sensor mismatches and parasitic effects. On the other hand, increasing the compensating slope, the dynamic response is reduced. Therefore, there is a trade-off between stability and dynamic response.

The main switch is turned on every cycle, thanks to a RS latch, and turned off when the control signal reaches the reference (Figure 2). Hence, this control technique prevents from the problem of variable frequency. The output capacitor current measurement provides fast dynamic response to load transitions since it behaves as a feed-forward of the load current and any change is instantaneously reflected in the control signal (Ctrl). When a positive load step occurs, the output capacitor current goes down almost immediately and therefore the control signal goes down as well. The duty cycle can be even saturated until the control signal reaches the reference again. On the other hand, the output error voltage feedback improves the dynamic response under changes in the output voltage reference as it is reflected in the control signal (Ctrl) and in the reference signal (Ref). Finally, the external voltage loop provides accurate steady state regulation.

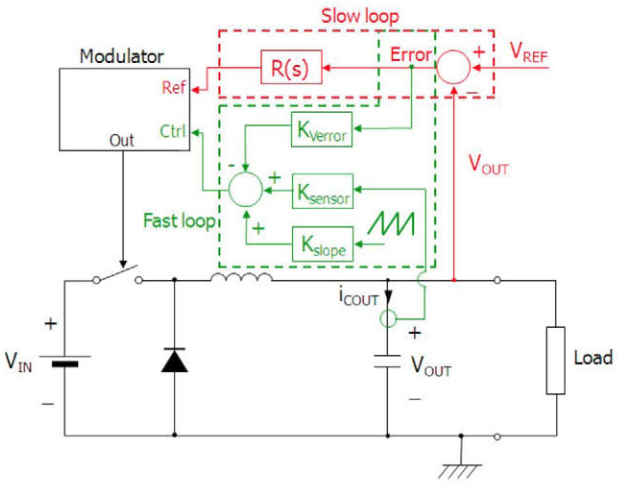

Figure 1. Proposed control technique: V^2I_C control.

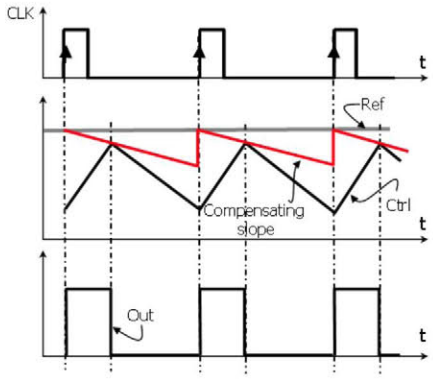

Figure 2. Proposed control: operating principle.

The operation of this control technique is experimentally validated on a buck converter being V_{IN}=3V, V_{OUT}=1V, f_{sw}=1MHz, L=440nH and C_{OUT}=4µF and the external voltage loop is designed with 10kHz bandwidth.

The dynamic response of the V^2I_C control under positive load step is shown in Fig. 3. The control reacts almost immediately closing the main MOSFET. The inductance current follows the reference with high slew rate. The recovery time is only 3µs (three switching cycles).

The experimental results obtained under positive reference step are shown in Fig. 4. The voltage reference step is done from 0.9V to 1.9V. The control reacts almost instantaneously needing only two switching cycles to reach the new operating point and then, the external voltage loop provides the accurate steady state regulation. In addition, there is no overshoot in the output voltage due to the transient response.

III. Comparison of the Proposed Control with Voltage Mode and Peak Current Mode Control

The control schemes that are compared in this paper are Voltage Mode control (Figure 5), Peak Current Mode Control (Figure 6) and V^2I_C control (Figure 1).

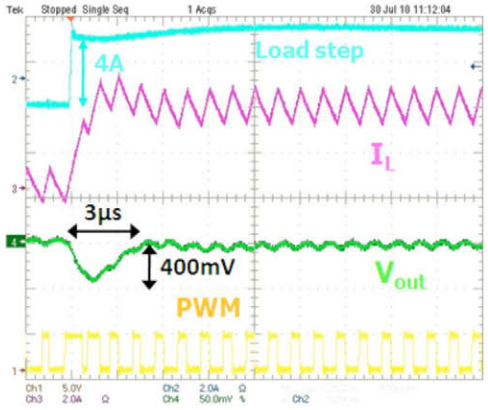

Figure 3. Experimental results. Positive load step of 4A and 40A/µs (2A/div), inductor current I_L (2A/div), output voltage V_{OUT} (500mV/div) and gate signal (5V/div) with 2µs/div time scale.

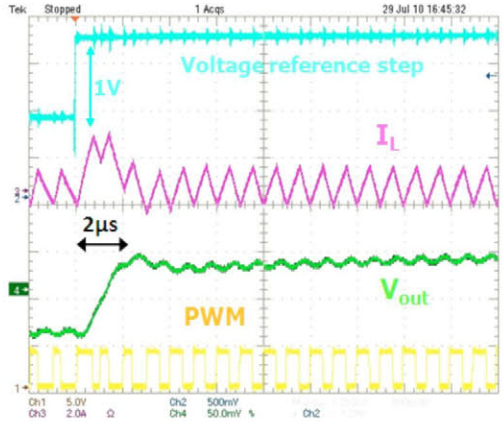

Figure 4. Experimental results. Positive voltage reference step of 1V and 20V/µs (500m/div), inductor current I_L (2A/div), output voltage V_{OUT} (500mV/div) and gate signal (5V/div) with 2µs/div time scale.

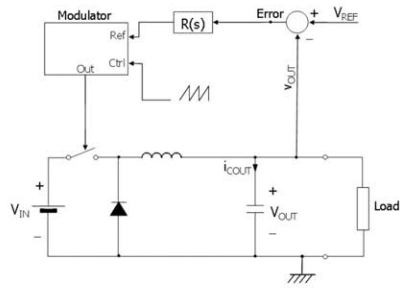

Figure 5. Voltage Mode Control (VMC)

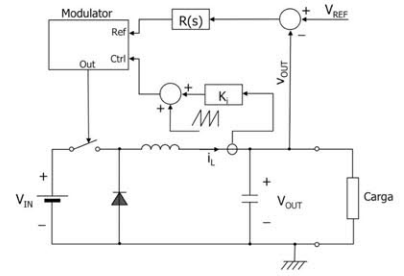

Figure 6. Peak Current Mode Control (PCMC)

These control techniques are applied to a Synchronous Buck converter with the following specifications: Input voltage range: 4V – 5.5V, output voltage: 1.2V – 2.2V, output current: 0A – 6A, switching frequency: 5MHz, output inductor: 100nH and output capacitor: 10μF (ESR=2mΩ, ESL=200pH).

The three control techniques have been modelled, designed and simulated with the simulation tool SIMPLIS. It allows to do both transient analysis and small signal analysis of switching converters. The VMC and the PCMC have been designed to have a voltage loop bandwidth of 500kHz. The reasons for 500kHz bandwidth are:

- It is one tenth of the switching frequency
- Robustness under additional output capacitors: the higher the bandwidth, the worse the stability under external capacitors added at the output.
- Robustness under parasitic variations: the resonance frequency of small ceramic capacitors is around 1.5MHz-3MHz. Since the loop gain is very sensitive to this resonance, the bandwidth should be far enough.

A. Open Loop Gain

In the V^2I_C control the selected bandwidth for the external voltage loop is 50 kHz. It is 10 times smaller than the bandwidth of VMC and PCMC since the dynamic response of this control is provided by the fast loop. Fig. 7 shows the open loop gain (magnitude and phase) for the three control techniques. The loop is designed for the nominal output capacitor (10μF). The phase margin is 70º in the three controls and the bandwidth is 50kHz in the V^2I_C control and 500kHz in the VMC and PCMC.

B. Closed Loop Output Impedance

Fig. 8 shows the corresponding closed loop output impedance for these three control techniques. It clearly shows that the V^2I_C control output impedance is much lower up to 1.8MHz; the fast internal loop of the V^2I_C control provides a really fast response with a 1.8MHz equivalent bandwidth, being only 50kHz the bandwidth of the slow external loop (voltage loop).

C. Dynamic Response

The dynamic response of the V^2I_C control is much faster than VMC and PCMC. Under load steps (Figure 9) the voltage deviation is 50mV while it is twice higher (100mV) in VMC or PCMC. Under reference voltage steps (Figure 10) the differences among the three controls are minor. V^2I_C control follows appropriately the reference step (185mV overshoot, 12μs settling time). The VMC follows also the step reference although it needs a higher settling time (20μs). The PCMC presents a higher overshoot (360mV).

D. Robustness: Extra Capacitors added at the Output

The V^2I_C control presents also very good performance under addition of extra capacitors at the output of the converter. Typically, the customer can add additional capacitors between the converter and the load and the system should be robust enough to handle the unknown additional capacitor without having stability problems. Fig. 11 shows the response of the three control techniques under a load step when the capacitor is 50 times higher than de nominal value. Fig. 12 shows the open loop gain of the three control techniques when the capacitor is 50 times higher than de nominal value. VMC has stability problems, the phase margin is only 11º and the response under the load step is too oscillating. PCMC is more robust to the capacitor variation but the bandwidth is too low (18kHz) and has a poor response under the load step, 65mV voltage deviation for such a big output capacitor (50 x 10μF). The V^2I_C control is very robust and keeps a stable behavior (39º phase margin) and a low voltage deviation (8mV) when the output capacitor is 50 times higher than the nominal value. The low bandwidth of the external voltage loop and the compensation slope provides the robustness of the V^2I_C control.

E. Line Regulation: Response under Input Voltage Steps

Fig. 13 shows the output voltage response under a voltage step at the input of the Buck converter. PCMC presents very good behavior since it has inherent feed-forward of the input voltage. V^2I_C control also presents very good response thanks to the fast internal loop. Finally, VMC presents a poor behavior under line steps.

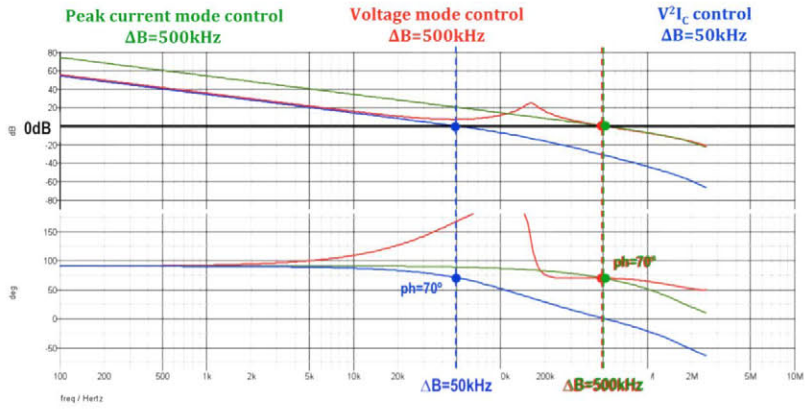

Figure 7. Open loop gain with the nominal output capacitor 10µF: Magnitude and phase

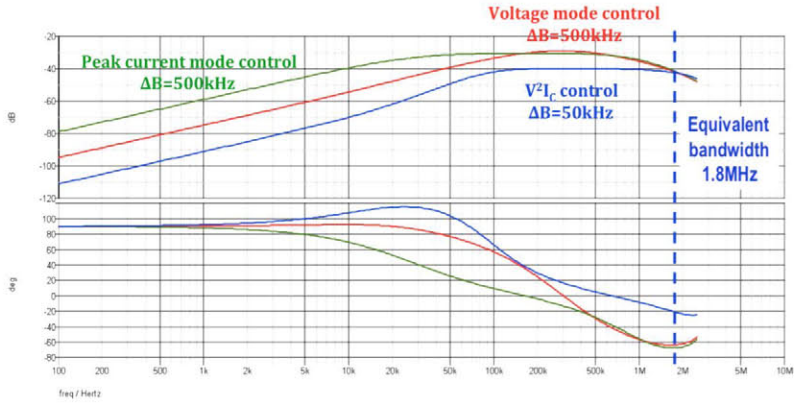

Figure 8. Closed loop output impedance (20dB/div) with the nominal output capacitor 10µF

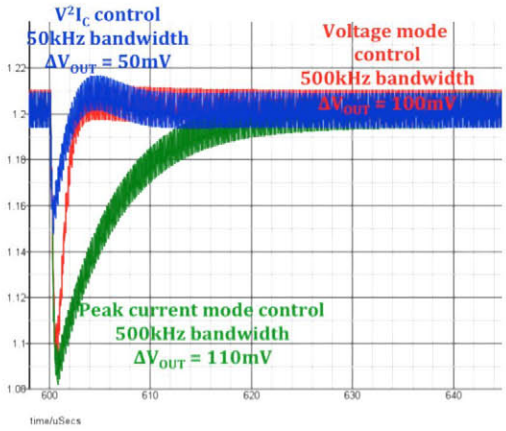

Figure 9. Output voltage response under a 4A load step with the nominal output capacitor 10µF (20mV/div, 10µs/div

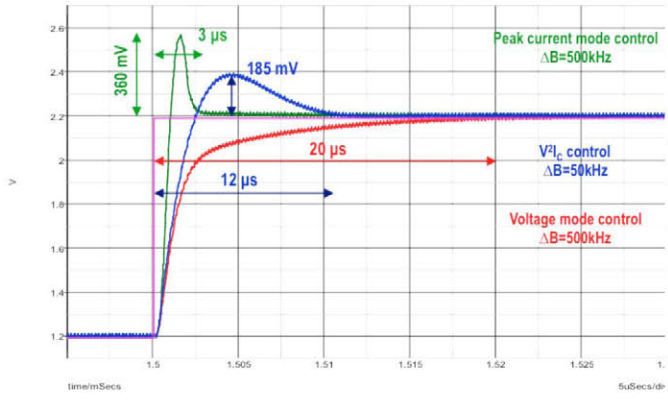

Figure 10. Reference voltage step: output voltage (0.2V/div) when the reference voltage steps from 1.2V to 2.2V with the nominal output capacitor 10µF (5us/div)

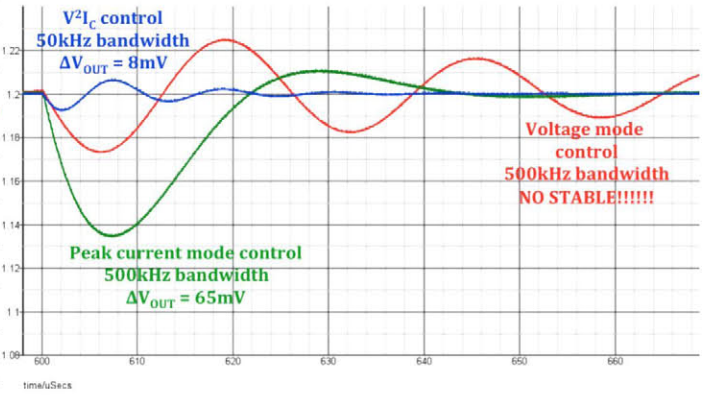

Figure 11. Output voltage response under a 4A load step being the output capacitor 50 x 10µF (20mV/div, 10µs/div)

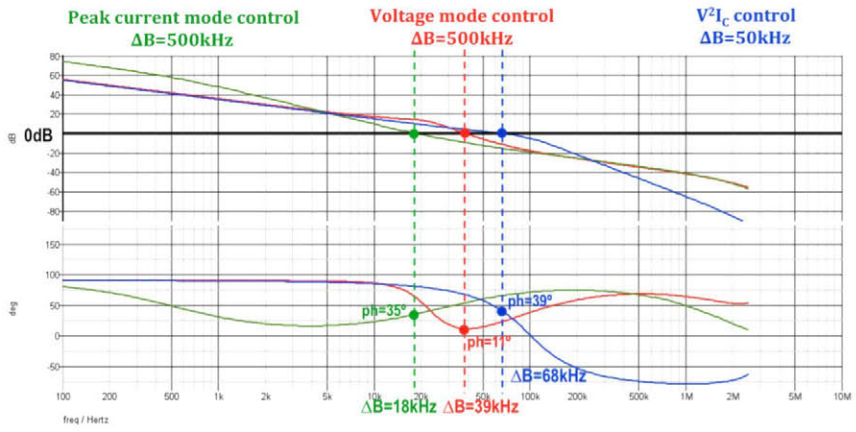

Figure 12. Open loop gain with an output capacitor 50 x 10µF: Magnitude and phase

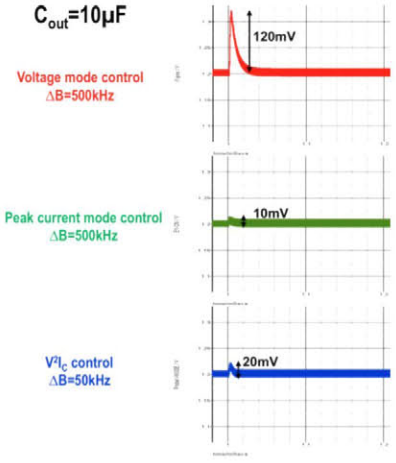

Figure 13. Line regulation: output voltage when the input voltage steps from 4V to 5.5V with the nominal output capacitor 10µF

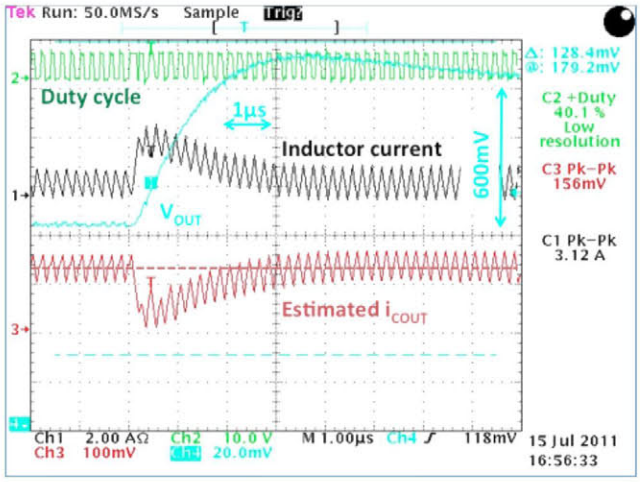

Figure 14. Experimental results: reference voltage step from 0.8V to 1.4V. Output voltage (200mV/div), estimated capacitor current (2A/div), inductor current (2A/div) and time scale 1us/div.

IV. Experimental Results

A 5MHz Buck converter has been developed to validate the behavior of the V^2I_C control. The prototype has been designed for the same specifications shown in section III. Fig. 14 shows the response of the V^2I_C control when the voltage reference steps from 0.8V up to 1.4V. The voltage step is appropriately followed, being the voltage overshoot about 100mV. Duty cycle is almost saturated during two cycles, increasing rapidly the current through the inductor and then the duty cycle is lowered to smoothly reduce the inductor current.

V. Conclusions

The V^2I_C control, based on two loops, a fast internal loop and a slow external loop, is very appropriate for high switching frequency converters. The low bandwidth of the external voltage loop together with the compensating slope provide a large robustness to this control. This control is presented and validated in [6].

In this paper, the V^2I_C control is compared with a high bandwidth Voltage Mode Control (VMC) and a high bandwidth Peak Current Mode Control (PCMC) for a 5MHz Buck converter. The comparison is done based on the SIMPLIS simulation tool. The three control techniques have been modeled, designed and simulated based on this tool.

The results of the comparison are summarized in the following table (Table I). The main conclusion of this paper is that the V^2I_C control, compared with VMC and PCMC, presents the fastest dynamic response as well as the best robustness to deal with additional output capacitors that the user can put between the load and the converter.

TABLE I. Summary of the Comparison

	Dynamic response under load steps	Dynamic response under reference voltage steps	Robustness under additional C_{OUT} (x50 times)	Closed loop Output impedance	Line regulation: Input voltage step
VMC 500kHz bandwidth	Fast response	Appropriate tracking (longer settling time)	UNSTABLE 11° phase margin	Medium	Worst response
PCMC 500kHz bandwidth	Fast response	Poor tracking (highest overshoot)	Stable but poor response	Highest	Best response
V2IC control 50kHz bandwidth	Very fast response	Appropriate tracking	Stable and fast response	Lowest (1.8MHz equivalent bandwidth)	Very good response

REFERENCES

[1] D. Goder and W. R. Pelletier, "V2 architecture provides ultra-fast transient response in switch mode power supplies", in Proceedings of HFPC Power Conversion 1996.

[2] J. Li and F. C. Lee, "Modeling of the V2 type current-mode control," in proc. IEEE Applied Power Electronics Conference APEC'09.

[3] Richard Redl and Jian Sun, "Ripple-Based Control of Switching Regulators—An Overview", in IEEE Transactions On Power Electronics, vol. 24, no. 12, December 2009.

[4] A. Soto, P. Alou and J.A. Cobos, "Non-Linear Digital control Breaks Bandwidth Limitations", in Proceedings of 2006 Applied Power Electronics Conference APEC '06.

[5] S.C. Huerta, P. Alou, J.A. Oliver, O. Garcia, J. A. Cobos, A. Abou-Alfotouh, "Design methodology of a non-invasive sensor to measure the current of the output capacitor for a very fast nonlinear control", IEEE Applied Power Electronics Conference APEC'09.

[6] M. del Viejo, P. Alou, J. A. Oliver, O. García, J. A. Cobos, "V2IC Control: a Novel Control Technique with Very Fast Response Under Load and Voltage Steps", IEEE Applied Power Electronics Conference APEC'11.

[7] G. K. Schoneman and D. M. Mitchell, "Output impedance considerations for switching regulators with current-injected control ", IEEE 1989.

[8] R. Redl et al., "Optimizing the Load Transient Response of the Buck Converter", in Proceedings of the IEEE Applied Power Electronics Conference APEC'98.

[9] M. del Viejo, P. Alou, J. A. Oliver, O. García, J. A. Cobos, "Fast control technique based on peak current mode control of the output capacitor current", IEEE Energy Conversion Congress and Exposition ECCE'10.